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A high speed embedded **cache design** with non-intrusive BIST - group of 2 »
S Kornachuk, L McNaughton, R Gibbins, B Nadeau- ... - Memory Technology, **Design** and Testing, 1994., Records of the ..., 1994 - ieeexplore.ieee.org
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Terms used **verification techniques for cache coherence**

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1 Verification techniques for cache coherence protocols

Fong Pong, Michel Dubois

March 1997 **ACM Computing Surveys (CSUR)**, Volume 29 Issue 1

Publisher: ACM Press

Full text available: pdf(1.25 MB) Additional Information: full citation, abstract, references, citings, index terms

In this article we present a comprehensive survey of various approaches for the verification of cache coherence protocols based on state enumeration, (symbolic model checking, and symbolic state models. Since these techniques search the state space of the protocol exhaustively, the amount of memory required to manipulate that state information and the verification time grow very fast with the number of processors and the complexity of the protocol mechanism ...

Keywords: cache coherence, finite state machine, protocol verification, shared-memory multiprocessors, state representation and expansion

2 The verification of cache coherence protocols

Fong Pong, Michel Dubois

August 1993 **Proceedings of the fifth annual ACM symposium on Parallel algorithms and architectures SPAA '93**

Publisher: ACM Press

Full text available: pdf(1.05 MB) Additional Information: full citation, references, citings, index terms

3 The STRESS method for boundary-point performance analysis of end-to-end multicast timer-suppression mechanisms

Ahmed Helmy, Sandeep Gupta, Deborah Estrin

February 2004 **IEEE/ACM Transactions on Networking (TON)**, Volume 12 Issue 1

Publisher: IEEE Press

Full text available: pdf(477.08 KB) Additional Information: full citation, abstract, references, citings, index terms

The advent of multicast and the growth and complexity of the Internet has complicated network protocol design and evaluation. Evaluation of Internet protocols usually uses random scenarios or scenarios based on designers' intuition. Such approach may be useful for average case analysis but does not cover *boundary-point* (worst or best case) scenarios. To synthesize boundary-point scenarios, a more systematic approach is needed.In this paper, we present a method for automatic synthesis of w ...

4 Modeling and validation of pipeline specifications

Prabhat Mishra, Nikil Dutt

Terms used **cache verification**

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1 Programming languages and object technologies: Verification caching: towards efficient and secure mobile code execution environments

Nael B. Abu-Ghazaleh, Dhananjay S. Phatak

March 2002 **Proceedings of the 2002 ACM symposium on Applied computing SAC '02**

Publisher: ACM Press

Full text available: pdf(443.31 KB) Additional Information: full citation, abstract, references, citings, index terms

In the mobile code paradigm for distributed systems (as well as in the active networks and agents frameworks), programs from possibly unknown hosts interact with the resources local to the host. While this model offers great potential, it also raises difficult security and performance issues. The mobile code unit should be guaranteed to be safe (not to abuse the resources of the host) in a limited time (since the acquisition of the code happens in real time --- e.g., a Java applet). Existing hos ...

2 Verification techniques for cache coherence protocols

Fong Pong, Michel Dubois

March 1997 **ACM Computing Surveys (CSUR)**, Volume 29 Issue 1

Publisher: ACM Press

Full text available: pdf(1.25 MB) Additional Information: full citation, abstract, references, citings, index terms

In this article we present a comprehensive survey of various approaches for the verification of cache coherence protocols based on state enumeration, (symbolic model checking, and symbolic state models. Since these techniques search the state space of the protocol exhaustively, the amount of memory required to manipulate that state information and the verification time grow very fast with the number of processors and the complexity of the protocol mechanism ...

Keywords: cache coherence, finite state machine, protocol verification, shared-memory multiprocessors, state representation and expansion

3 The verification of cache coherence protocols

Fong Pong, Michel Dubois

August 1993 **Proceedings of the fifth annual ACM symposium on Parallel algorithms and architectures SPAA '93**

Publisher: ACM Press

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4 Verification of FLASH cache coherence protocol by aggregation of distributed transactions

Terms used **cache verification random**

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1 Functional verification of a multiple-issue, out-of-order, superscalar Alpha processor—the DEC Alpha 21264 microprocessor

Scott Taylor, Michael Quinn, Darren Brown, Nathan Dohm, Scot Hildebrandt, James Huggins, Carl Ramey

May 1998 **Proceedings of the 35th annual conference on Design automation DAC '98**

Publisher: ACM Press

Full text available: pdf(153.68 KB) Additional Information: full citation, abstract, references, citings, index terms

DIGITAL's Alpha 21264 processor is a highly out-of-order, superpipelined, superscalar implementation of the Alpha architecture, capable of a peak execu tion rate of six instructions per cycle and a sustainable rate of four per cycle. The 21264 also features a 500 MHz clock speed and a high-bandwidth system interface that channels up to 5.3 Gbytes/second of cache data and 2.6 Gbytes/second of main-memory data into the processor. Simulation-based functional verification was performed on the lo ...

Keywords: 21264, Alpha, architecture, coverage anaysis, microprocessor, pseudo-random, validation, verification

2 A BNF-based automatic test program generator for compatible microprocessor verification

Lieh-Ming Wu, Kuochen Wang, Chuang-Yi Chiu

January 2004 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 9 Issue 1

Publisher: ACM Press

Full text available: pdf(306.47 KB) Additional Information: full citation, abstract, references, citings, index terms

A novel Backus-Naur-form- (BNF-) based method to automatically generate test programs from simple to complex ones for advanced microprocessors is presented in this paper. We use X86 architecture to illustrate our design method. Our method is equally applicable to other processor architectures by redefining BNF production rules. Design issues for an *automatic program generator* (APG) are first outlined. We have resolved the design issues and implemented the APG by a *top-down recursive de ...*

Keywords: *Advanced microprocessor, BNF, automatic program generator, compatibility verification, coverage, top-down recursive descent parsing method*

3 Cache performance analysis of traversals and random accesses

Richard E. Ladner, James D. Fix, Anthony LaMarca

January 1999 **Proceedings of the tenth annual ACM-SIAM symposium on Discrete algorithms SODA '99**

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Roth, A.; Ronen, R.; Mendelson, A.;
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Wunderlich, J.T.;
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